Notice of Allowability	Application No.	Applicant(s)	
	10/649,765	OBARA, TERUHISA	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/27/07*.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4/30/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Applicant's response was received and entered March 27, 2007.

- Claims 1-12 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: The prior art of record does not teach the following limitations:

The present invention teaches a semiconductor integrated circuit having an operational mode for processing operation input data and a test mode for processing test input data, comprising: a plurality of scan registers that are operable in response to a clock signal and a mode signal, each scan register having an output terminal, an operation input data terminal, and a test input data terminal; a plurality of logic circuits, each having an input terminal and having an output terminal that is connected to the operation input data terminal of one of the scan registers, the logic circuits and the scan registers being connected alternately in series to form m scan chains (wherein m is an integer greater than 1), the scan chains being connected to one another in a sequence, each of the scan chains including a first logic circuit: a first scan register connected to the first logic circuit a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains, the serial/parallel conversion circuit converting serial test input data supplied during the test mode into parallel test input data in response to a multiplied clock signal having a frequency that is m times that of the clock signal, the parallel test input data being fed in parallel to the scan chains; and a parallel/serial conversion circuit connected to the output terminals of the

last scan registers of the scan chains, the parallel/serial conversion circuit converting parallel data received from the scan chains into serial data in response to the multiplied clock signal, wherein the parallel/serial conversion circuit comprises a selector that receives the clock signal and selectively outputs processed test input data from the last scan registers of the scan chains in response to the clock signal during the test mode, and a flip-flop that receives the multiplied clock signal and latches output data from the selector in response to the multiplied clock signal wherein operation input data is supplied to the sequence of scan chains via the input terminal of the first logic circuit in a first one of the scan chains in the operational mode, and wherein the flip-flop outputs processed operation input data from the sequence of scan chains during the operational mode, in claim 1 and 7.

The prior arts of record Whetsel et al. US Pat no. 6,242,269 B1 and Eriksson et al. US Pat no. 6,169,500 do not teach the structure of the semiconductor integrated circuit as taught in claims 1 and 7. Whetsel teaches an integrated circuit having parallel scan paths includes a pair or pairs of scan distributor and scan collector circuits. The scan paths apply stimulus test data to functional circuits on the integrated circuit and receive response test data from the functional circuits. A scan distributor circuit receives serial test data from a peripheral bond pad and distributes it to each parallel scan path. A scan collector circuit collects test data from the parallel scan paths and applies it to a peripheral bond pad. However, Whetsel fails to teach the exact structure of the circuit as in claims 1 and 7. Further, Whetsel fails to teach the connections of logic circuits and scan chains and the scan chains are not connected to each other in a

sequence as claimed in claims 1 and 7. Eriksson teaches fast serial-parallel and parallel-serial converters, and in them included frequency dividers. However, Eriksson fails to overcome the structural differences between Whetsel and claims 1 and 7.

Hence, the prior arts of record fail to anticipate or render obvious the claimed inventions. Thus claims 1-12 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

/Cynthia Britt/
Primary Examiner
AU 2117 6/15/07

Saqib Siddiqui